AMENDMENT TO THE CLAIMS

Claims 1-79. (Canceled)

80. (Previously presented) A processor for operating on certain data in accordance with an instruction in a program, said instruction designates a first register or a second register, said processor comprising:

a first unit configured to perform sign-extending of the certain data if the instruction designates the second register; and

a second unit configured to perform zero-extending of the certain data if the instruction designates the first register.

81. (Previously presented) The processor of Claim 80, wherein the instruction includes a destination operand which designates said first register or said second register.

82. (Previously presented) The processor of Claim 81, wherein said data is an immediate data included in the instruction.

83 and 84. (Canceled)

85. (Currently amended) A processor-implemented data processing method for executing an instruction in a program, said instruction designates a first register or a second register, said method comprising:

decoding the instruction;

performing zero-extending of data if the instruction designates the first register; and

performing sign-extending of data if the instruction designates the second register.

86. (Canceled)

87. (Currently amended) The processor-implemented data processing method of Claim 85, wherein said data is an immediate data included in the instruction.

88. (Previously presented) A processor for operating on certain data in accordance with an instruction in a program, said instruction designating a first register or a second register, said processor comprising:

a first register unit;

a second register unit; and

a processing unit configured to perform zero-extending of the certain data if the instruction designates the first register, and to perform sign-extending of the certain data if the instruction designates the second register.

89. (Previously presented) The processor of Claim 88, wherein the instruction includes a destination operand which designates either the first register or the second register.

90. (Previously presented) The processor of Claim 89, wherein the data is an immediate data.

91-94. (Canceled)

95. (Currently amended) The processor-implemented data processing method of Claim 85, wherein the instruction includes a destination operand which designates said first register or said second register.